

20.1 A 40nm CMOS Receiver for 60GHz Discrete-Carrier Indoor Localization Achieving mm-Precision at 4m Range

Tom Redant, Tuba Ayhan, Nico De Clercq, Marian Verhelst, Patrick Reynaert, Wim Dehaene

KU Leuven, Leuven, Belgium

The globally available large unlicensed frequency spectrum around 60GHz has recently gained a lot of attention. Its broad bandwidth, combined with a high allowed transmitted power level, provides an excellent opportunity for numerous applications, among others high-precision ranging and localization. Despite being readily available at 60GHz, high bandwidths come with a significant power penalty in the baseband. The presented work brings a solution that delivers high ranging precision at heavily reduced processing bandwidths and sparse-bandwidth power allocations.

Classic ToA ranging and localization applications, such as FMCW, wideband equivalent-time sampling and successive-approximation radar (SAR), use single-carrier (SC) schemes [1-3] with power spread over a wide bandwidth to achieve precision. Moreover, they often require TX-RX carrier phase-locking (homodyne detection), which in its turn comes at a severe system complexity and thus energy cost. [4] shows that a less-dense power allocation by means of multiple discrete tones does not reduce the performance of a ranging system significantly with respect to a fully occupied bandwidth. This opens doors to wideband OFDM-like signal structures, easy to generate in TX and optimizable for a low crest factor to increase transmitter efficiency. Moreover, multi-tone frequency domain multiplexing instead of time-domain multiplexing as in FMCW [1] and SAR [2] enables higher update rates. Last but not least, the multi-tone approach enables smart signal sub-sampling for maximum efficiency with negligible precision loss, as exploited here.

The System's block diagram is presented in Fig. 20.1.1, top. The multi-tone 1.56GHz bandwidth, 60GHz burst is first processed by a wide bandwidth on-chip direct downconversion receiver front-end [5], resulting in a wideband quadrature baseband signal. Before digitization, all I/Q decomposed tones are folded to a small bandwidth of 60MHz by means of sub-sampling as shown in Fig. 20.1.1, right. The sub-sampling frequency is adjustable by division of the receiver's system clock of 3GHz by a sub-sampling factor, varying between 1 (for no subsampling) and 32. After sub-sampling, the frequency-folded I/Q signal is digitized at low rate [6]. The digitized data is then ready to be processed by the ToA estimation algorithm.

The time-based range-estimation algorithm [4] is based on detecting the value of the phase shifts of each of the discrete signal tones. As illustrated in Fig. 20.1.1 (left) the sub-sampling factor does not change the phases of the tones. Even sampling rates below Nyquist rate (2 times signal bandwidth, 2xB) can be used, provided a careful frequency planning of the multi-tone ranging measurement signal ensures the tones are folded to non-overlapping frequencies after sub-sampling. These frequency-folded tones hence preserve the information as provided by their original tones, enabling reconstruction of the original signal in the digital domain. However, this comes at the unavoidable penalty of aliased out-of-band noise, decreasing SNR. However, SNR loss is largely compensated by the advantage of the higher signal bandwidth that can be digitized using the technique: A typical noise-corrupted ranging system's precision, defined as the RMS value of distance estimation, is inversely proportional to $SNR^{1/2}$ and $B^{3/2}$ [4], shown theoretically and experimentally in Fig. 20.1.2 (top left). As confirmed by measurements (stars in figure), a 20x sub-sampling system can provide over a magnitude more precise estimations compared to a Nyquist rate system with identical bandwidth after sampling and similar complexity.

Figure 20.1.3 provides details on the IC. The 60GHz burst is first amplified by a wide bandwidth LNA followed by quadrature downconversion mixers, having a high bandwidth of 4GHz [5]. The LNA uses a fully differential 2-stage topology. Transformers are employed to perform the single-ended to differential conversion at the input, to couple both stages and to couple the LNA to the mixers. Matching is achieved by slow-wave transmission lines (SWTL), placed in series with the transformers. The combination of transformers and SWTL's allows for a good impedance match across a wide bandwidth. A double-balanced mixer topology is used to achieve a better port-to-port isolation and higher suppression of spurious mixing products. The quadrature LO signals, driving the downconversion mixers, are generated by means of an on-chip poly-phase filter (PPF). A cascade of 2 PPFs is used to obtain a good I/Q phase relationship,

resilient to CMOS processing variations. Buffers, employing capacitive gate-drain neutralization, are used to compensate for the high insertion loss caused by the PPF. The downconverted differential signals are applied directly to the sub-sampling stage.

The sub-sampling is carried out by means of a wideband transmission gate and a MOM S&H capacitor. After amplification and AC-coupling, the folded signal is forwarded to the I/Q ADC. The dual ADC is an open-loop VCO-based topology, shaping quantization noise to higher frequencies, as is beneficial after the bandwidth reduction operation. The ADC uses internal AC coupling to set the VCO's input common mode close to the rail, improving linearity. The VCO's state is sampled at the receiver's system clock of 3GHz. This high clock frequency enables suppression of the ADC's quantization noise. The digital samples of a signal burst are stored in an on-chip 96kB SRAM memory, accessible by the ToA estimation algorithm.

The circuit was processed in a general purpose 0.9V 40nm CMOS technology (Fig. 20.1.7). The entire receiver has a total area of 2.93mm². The indoor lab-measurement setup is shown in Fig. 20.1.4. The transmitted tones, equal in power and phase, are generated at an IF by means of a Tektronix AWG. A Siivers IMA converter module takes care of upconversion to 60GHz and power amplification. Millitech SGH-15 Horn antennas are employed to transmit and receive the signal. An external 40dB LNA is added, compensating for channel attenuation effects and limited transmit power. LNA addition enables measuring the performance as limited by the IC and not by channel or transmitter.

Six discrete tones are transmitted at frequencies [59.22 59.6 59.8 60.2 60.4 60.78]GHz. The exact carrier allocation or phase may change in order to optimize the crest factor. The transmitted signal's crest factor is calculated to be 7.8dB. The total chip input power at 80cm separation equals -2.8dBm. Due to measurement setup non-linearities, the SFDR of the signal at the receiver's input is only 15.5dB. Sampled at 187.5MHz (subsampling factor 16), the discrete tones frequency-fold to the frequencies [-30.029 -20.142 -10.253 0.253 20.142 30.029] MHz. Wireless measurements are performed at different distances between transmitter and receiver, varying between 1m and 5m. At each distance, 60 measurements using a multi-tone 4μs burst are performed. After synchronization, the frequency domain representations of multiple bursts are added to further average out channel noise, drastically improving precision. The measured estimation precision and accuracy (mean value of the estimation error) using statistical averaging with 5 burst combinations (20μs packages) is plotted in Fig. 20.1.5, demonstrating overall cm-level precision, enabling a 50kHz update rate. Precisions in the order of a few millimeters are even achieved at 3.6 meter distance.

Figure 20.1.6 compares the design to state-of-the-art CMOS implementations of ranging receivers. Power consumption of the IC is measured to be 195mW during reception and 166mW in idle mode, excluding the SRAM modules which only serve for measurement purposes. This comparison clearly shows that sub-cm-precision, high-update-rate ranging can be achieved, based on wideband discrete tones around 60GHz. This performance is competitive to state-of-the-art, with the additional strong advantage of not requiring a fixed TX-RX LO phase relation nor baseband circuits with excessive bandwidth requirements.

Acknowledgements:

This work was funded and assisted by The Flemish Agency for Innovation by Science and Technology (IWT) and ERC Advanced Grant DARWIN. Thanks to FMTC Leuven, F. Daenen, N. Gaethofs and N. Deferm.

References:

- [1] Lee et al., "A Fully-Integrated 77GHz FMCW Radar Transceiver in 65nm CMOS Technology," *IEEE J. Solid-State Circuits*, 2010.
- [2] Tang et al., "A 144GHz 0.76cm-Resolution Sub-Carrier SAR Phase Radar for 3D Imaging in 65nm CMOS," *ISSCC Dig. Tech. Papers*, 2012.
- [3] Lai et al., "A Scalable Direct-Sampling Broadband Radar Receiver Supporting Simultaneous Digital Multibeam Array in 65nm CMOS," *ISSCC Dig. Tech. Papers*, 2013.
- [4] T. Ayhan et al., "Towards a Fast and Hardware-Efficient sub-mm Precision Ranging System", *IEEE Workshop on Signal Processing Systems (SIPS)*, pp. 203-208, 2012.
- [5] N. De Clercq et al., "A 60GHz Wideband Direct Downconversion Receiver in 40nm CMOS", *European Microwave Integrated Circuits Conference (EUMIC)*, October 2013, Accepted.
- [6] T. Redant and W. Dehaene, "A 40nm, High-Bandwidth, VCO-based Burst-Mode Receiver Backend for EHF Multi-Carrier Wireless", accepted for publication at A-SSCC 2013.

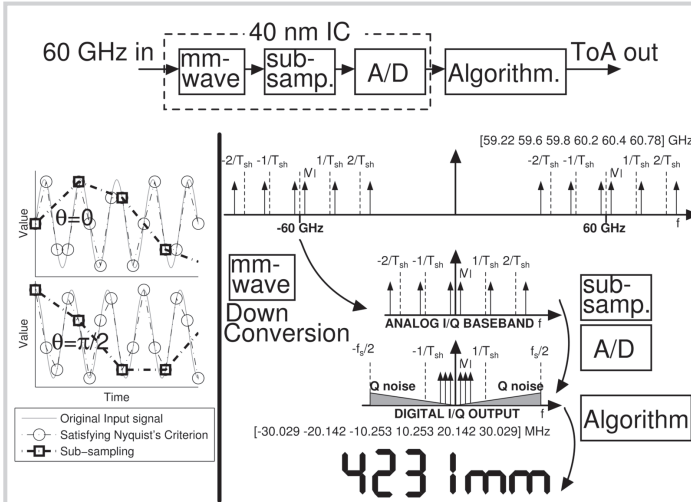


Figure 20.1.1: Core building blocks (top) and functionality of the IC + algorithmic processing. Explanation of the sub-sampling in both time (bottom left) and frequency domain (bottom right).

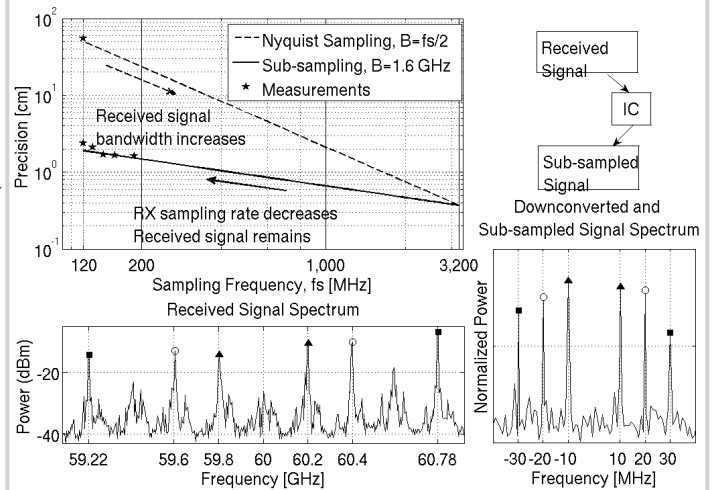


Figure 20.1.2: Impact of sampling rate and signal bandwidth on the range-estimation precision.

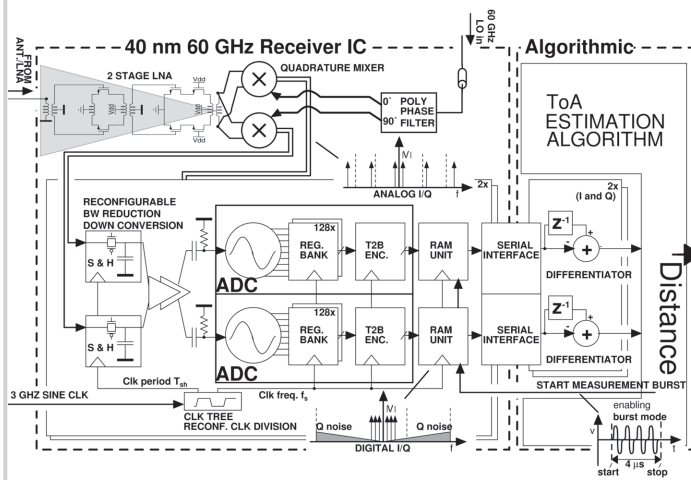


Figure 20.1.3: System block diagram overview. The IC is represented by the dashed box on the left.

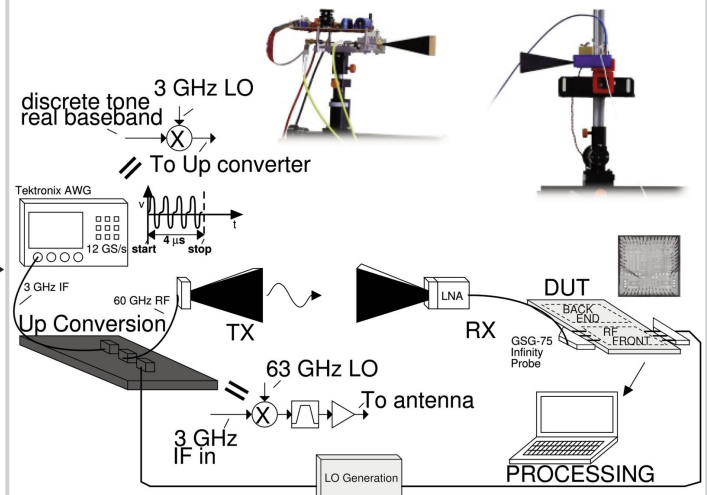


Figure 20.1.4: 60GHz discrete-tone ranging setup. Left: Transmitter + antenna, Right: DUT and receive antenna + LNA. Data is transferred by means of an Agilent ParBERT 81250 system to the algorithm.

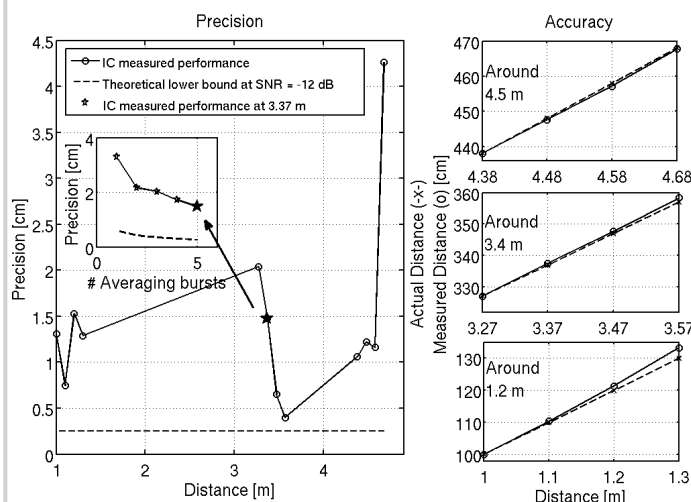


Figure 20.1.5: Measured performance of the ToA-based ranging IC setup: precision and absolute accuracy.

	This Work	[1] (JSSC2010)	[2] (ISSCC2012)	[3] (ISSCC2013)
Features	Multi-tone, bandwidth-reducing	FMCW	SAR frequency sweep	Equivalent time-sampling
Max measured range	5m	≈100m	1.2m	N/A
Precision (RMS value)	4mm @ 3.6m (measured)	< 100mm @ 10 m (measured)	7.6mm @ >1m (measured)	Depth resolution 1.5 mm (theoretical)
Receiver Power Consumption	195mW	> 100mW	214mW	76mW
Frequency Band	60GHz (V-band)	77GHz (W-band)	144GHz (D-band)	10GHz
Bandwidth	2GHz	700MHz	400MHz	5.4GHz
Package Duration (Integration time)	20μs	1.5ms	2μs	1.5μs
Signal Type	Multi-Tone	FMCW-sweep	Single Tone	Wideband
Tx-Rx LO phase relation theoretically needed?	NO	NO	YES	YES
Usage of external LO	YES	NO	NO	NO
CMOS Tech.	40nm	65nm	65nm	65nm

Figure 20.1.6: Comparison table. Sub-cm-precision high-update-rate ranging can be achieved, based on the wideband discrete tones around 60GHz that were employed, though the baseband bandwidth is small.

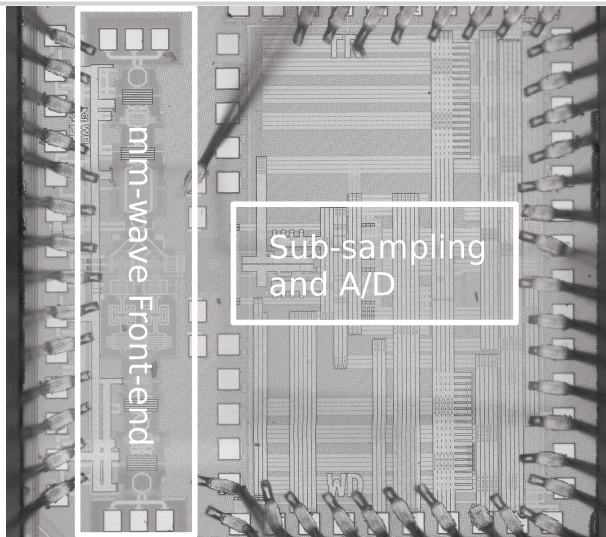


Figure 20.1.7: Micrograph of the 40 nm IC realization. Total chip size: 2.93 mm².